

**Notice of Allowability**

Application No.

10/634,857

Applicant(s)

ARAKAWA, TOSHIO

Examiner

Binh C. Tat

Art Unit

2825

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.


1. ☒ This communication is responsive to 09/16/04.
2. ☒ The allowed claim(s) is/are 1,3-5,8 and 9.
3. ☒ The drawings filed on 09/16/04 are accepted by the Examiner.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some\* c) ☐ None of the:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).  
\* Certified copies not received: \_\_\_\_\_.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.  
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.  
(a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached  
1) ☐ hereto or 2) ☐ to Paper No./Mail Date \_\_\_\_\_.  
(b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date \_\_\_\_\_.  
Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

- |   |   |
|---|---|
| 1. <input type="checkbox"/> Notice of References Cited (PTO-892)  | 5. <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)           |
| 2. <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                | 6. <input type="checkbox"/> Interview Summary (PTO-413),<br>Paper No./Mail Date _____ |
| 3. <input type="checkbox"/> Information Disclosure Statements (PTO-1449 or PTO/SB/08),<br>Paper No./Mail Date _____ | 7. <input type="checkbox"/> Examiner's Amendment/Comment                              |
| 4. <input type="checkbox"/> Examiner's Comment Regarding Requirement for Deposit<br>of Biological Material          | 8. <input checked="" type="checkbox"/> Examiner's Statement of Reasons for Allowance  |
|   | 9. <input type="checkbox"/> Other _____   |

  
VUTHE SIEK  
PRIMARY EXAMINER

## **DETAILED ACTION**

### ***Reasons for Allowance***

The following is an examiner's statement of reasons for allowance:

Claims 1, 3-5, 8, and 9 are allowed because the prior art does not teach or suggest a design method for an integrated circuit having a logic circuit, comprising: fourth step of generating a fifth netlist, from a fourth netlist that includes the second flip flops, and scan chain interconnects that depend on the scan-chain interconnect order data, by substituting the second flip flops for a plurality of standard cells, and of performing layout of the standard cells and interconnects thereof which are contained in the fifth netlist, in accordance with the fifth netlist; and a step of generating logic circuit test patterns on the basis of the fourth netlist, wherein: the standard cells are registered in a layout library as hard macros that contain layout information, and the layout of the standard cells is performed in the fourth step with reference to the layout library, and the second flip flop having the scan function is not registered in the layout library as a hard macro that contains layout information.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance".

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***Conclusion***


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Binh Tat whose telephone number is (703) 305-4855. The examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Tat Binh

Patent Examiner

September 28, 2004

  
**VUTHE SIEK**  
**PRIMARY EXAMINER**